Remarks

Applicants respectfully request reconsideration of this application as new. Claims 1, 5, 8, 9, 16 and 20 have been amended. Claims 4 and 21-24 have been canceled. No new claims have been added. Therefore, claims 1-3 and 5-20 are presented for examination.

In a Final Office Action, mailed August 12, 2003, claims 1-3 and 8-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hetherington, et al., U. S. Patent 5,978,864 in view of Shiell, et al, U.S. Patent 6,138,232. Applicants submit that the present claims are patentable over Hetherington in view of Shiell.

Hetherington discloses a system and method for thermal overload detection and protection for an integrated circuit processor. The system allows the processor to run at near maximum potential for the vast majority of its execution life. This is effectuated by the provision of circuitry to detect when the processor has exceeded its thermal thresholds and which then causes the processor to automatically reduce the clock rate to a fraction of the nominal clock while execution continues. When the thermal condition has stabilized, the clock may be raised in a stepwise fashion back to the nominal clock rate. See Hetherington at col. 3, ll. 53-65.

Shiell discloses a method of operating a microprocessor. The microprocessor accepts an interrupt from one of a plurality of interrupt sources. The microprocessor then operates at a rate dependent upon the interrupt source. The rate of power consumption by the microprocessor corresponds to the selected rate of instruction operation. A rate table stores a table of interrupt source to rate of instruction operation. The rate table is accessed upon receipt of an interrupt to obtain a rate of instruction operation

corresponding to the interrupt source. The microprocessor is then operated at the recalled rate. The rate table may be a read only memory or a read/write memory loaded upon initiation of the microprocessor. The rate of instruction operation may be controlled by a rate of instruction dispatch. For a superscalar microprocessor capable of concurrently executing plural instructions simultaneously the rate of instruction operation may be set by setting a number of instructions dispatched per instruction cycle. This could include dispatching instructions to a number of execution units based upon the selected rate. Electric power consumption is conserved by powering only those execution units to which instructions are dispatched. See Shiell at col. 1, ll. 45 – col. 2, ll. 25.

Claim 1 recites programmable array logic (PAL) to operate as an interrupt handler to control a CPU upon receiving an interrupt. Applicants submit that there is no disclosure in Hetherington or Shiell of programmable array logic (PAL) to operate as an interrupt handler to control a CPU upon receiving an interrupt.

Since neither Hetherington nor Shiell disclose or suggest programmable array logic (PAL) to operate as an interrupt handler to control a CPU upon receiving an interrupt, any combination of Hetherington and Shiell would also not disclose or suggest such a feature. Accordingly, claim 1 is patentable over Hetherington in view of Shiell.

Claims 2-3 and 5-7 depend from claim 1 and contain additional features. Thus, claims 2-3 and 5-7 are also patentable over Hetherington in view of Shiell.

Claim 8 recites receiving an interrupt at programmable array logic (PAL), wherein the PAL controls a CPU upon receiving the interrupt.

Thus, for the reasons described above with respect to claim 1, claim 8 is also patentable over Hetherington in view of Shiell. Since claims 9-15 and 20 depend from

claim 8 and contain additional features, claims 9-15 and 20 are also patentable over Hetherington in view of Shiell.

Claim 16 recites an instruction execution unit to receive a signal from programmable array logic (PAL) indicating execution of a first quantity of instructions per cycle in a first execution mode whenever a thermal sensor measures temperature exceeding a predetermined threshold.

Thus, for the reasons described above with respect to claim 1, claim 16 is also patentable over Hetherington in view of Shiell. Since claims 17-19 depend from claim 16 and contain additional features, claims 17-19 are also patentable over Hetherington in view of Shiell.

Claims 4-7 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hetherington in view of Shiell and further in view of McFarland et al., U.S. Patent 5,125,093. Applicants submit that the present claims are patentable over any combination of Hetherington, Shiell and McFarland.

McFarland discloses a technique of servicing interrupts among a plurality of microprocessors. See McFarland at Abstract. Nevertheless, McFarland does not disclose or suggest programmable array logic (PAL) to operate as an interrupt handler to control a CPU upon receiving an interrupt.

As discussed above, neither Hetherington nor Shiell disclose or suggest such a limitation. Therefore, any combination of Hetherington, Shiell and McFarland would also not disclose or suggest programmable array logic (PAL) to operate as an interrupt handler to control a CPU upon receiving an interrupt.

Applicants respectfully submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Respectfully submitted,

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Date: March 16, 2005

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